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10/802,481	03/16/2004	Ronald N. Perry		4085

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EXAMINER	
WASHBURN, DANIEL C	
ART UNIT	**PAPER NUMBER**
2628	

Patent Department
Mitsubishi Electric Research Laboratories, Inc.
201 Broadway
Cambridge, MA 02139

DATE MAILED: 03/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/802,481	PERRY ET AL.
	Examiner	Art Unit
	Dan Washburn	2628

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 25 July 2005.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-23 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 16 March 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 6/20/05.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments, see pages 7-11, filed 7/25/05, with respect to the rejection(s) of claim(s) 22 and 23 under Hussain (US 6,801,203) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Gaudette et al. (US 6,867,782).

Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

Double Patenting

Claims 22 and 23 of this application conflict with claims 1 and 14 of Application No. 10/802,468. 37 CFR 1.78(b) provides that when two or more applications filed by the same applicant contain conflicting claims, elimination of such claims from all but one application may be required in the absence of good and sufficient reason for their retention during pendency in more than one application. Applicant is required to either cancel the conflicting claims from all but one application or maintain a clear line of demarcation between the applications. See MPEP § 822.

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in

scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claims 22 and 23 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1 and 14 of copending Application No. 10/802,468. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

The following table compares the limitations found in claim 22 of this application against the limitations found in claim 14 of copending Application No. 10/802,468 (Perry).

Claim 22 of this application.	Claim 14 of Application No. 10/802,468
An apparatus for rendering, comprising: means for querying a progressive cache to determine a cached element most representing a display image satisfying a rendering request for an object;	An apparatus for processing data, comprising: means for querying a progressive cache to determine a cached element most representing an output satisfying a processing request for input data;
means for sending the cached element to a starting stage of a rendering pipeline for the object, the starting stage associated with the cached element; and	means for sending the cached element to a starting stage of a processing pipeline for the data, the starting stage associated with the cached element; and
means for sending an output of the starting stage to an input of a next stage of the	means for sending an output of the starting stage to an input of a next stage of the

rendering pipeline, a final stage of the rendering pipeline determining the display image satisfying the rendering request.	processing pipeline, a final stage of the processing pipeline determining the output satisfying the processing request for the input data.

As the table illustrates, claim 22 of this application describes rendering a display image based on a rendering request. Claim 14 of Perry describes processing an output based on a processing request. 'Rendering' and 'processing', 'output' and 'display image', and 'object' and 'input data' are considered to be equivalent, respectively, in the above context. In each case a progressive cache is queried, cached elements are sent to a starting stage of a pipeline, and the output of the starting stage acts as the input to a next stage in the pipeline, a final stage determining the output, or display image, satisfying the rendering, or processing, request for an object, or input data. The two sets of limitations are considered equivalent.

The following table compares the limitations found in claim 23 of this application against the limitations found in claim 1 of copending Application No. 10/802,468 (Perry).

Claim 23 of this application.	Claim 1 of Application No. 10/802,468
A system for rendering, comprising: a rendering pipeline including a plurality of stages connected serially to each other so that output of a previous stage provides input to a next stage, and a first stage is	A system for processing data, comprising: a processing pipeline including a plurality of stages connected serially to each other so that an output element of a previous stage is sent as an input element to a next

configured to receive a rendering request for an object, and a last stage is configured to produce a display image corresponding to the object;	stage, and a first stage is configured to receive input for a processing request, and a last stage is configured to produce output corresponding to the input;
a progressive cache including a plurality of caches arranged to store cached elements in a least finished to a most finished order; and	a progressive cache including a plurality of caches arranged in an order from least finished cache elements to most finished cache elements, each cache for receiving an output cache element of a corresponding stage and for sending an input cache element to a next stage after the corresponding stage; and
a cache controller configured to route a most finished cache element from the progressive cache to a next stage of a corresponding stage of the rendering pipeline and the output of a stage of the rendering pipeline to a corresponding cache of the progressive cache.	a cache controller configured to route cache elements from the processing pipeline to the progressive cache in the order from a least finished cache element to a most finished cache element and from the progressive cache to the processing pipeline in the order from the most finished cache element to the next stage after the corresponding stage.

As the table illustrates, claim 23 of this application describes producing a displayed image based on an object rendering request. Claim 1 of Perry describes producing an output based on an input processing request. 'Rendering' and 'processing', 'output' and 'display image', and 'object' and 'input' are considered to be equivalent, respectively, in the above context. The described pipelines, caches, and cache controllers are considered to be functionally equivalent. The serially connected pipelines receive a request for processing at the first stage and produce an output at the last stage, the progressive caches store cache elements in a least finished to most finished order, and the cache controllers route cache elements from the pipeline to a corresponding stage of the progressive cache, which is considered routing from a least finished cache element to a most finished cache element, and route the most finished progressive cache element to a next stage of a corresponding stage of the pipeline. The two sets of limitations are considered equivalent.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting

directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-3, 12, 14, 15, and 21-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Gaudette et al. (US 6,867,782).

As to claim 1, Gaudette describes a method for rendering, comprising: defining a rendering request, the rendering request describing an object to be rendered in a single rendering pipeline including a plurality of stages connected serially to each other so that output of a previous stage provides input to a next stage (column 1 lines 66-67, column 2 lines 1-17, and Figure 6 describe a processing, or rendering, pipeline. Figure 6 illustrates input clips 603 through 606 and processing stages 607 through 610, which are configured to receive input clips 603 through 606 upon receipt of an input frame request, processing stages 609, 612, 613, and 602, which are connected serially to each other so that an output element of a previous stage is sent as an input to the next stage, and stage 601, which is configured to produce an output corresponding to the input. Column 4 lines 37-45 describes that when a user composites a complex scene, the user will import film material digitally, possibly from a variety of sources. If the user imports film from one source, as described, then all the rendering will take place in a single pipeline); querying a progressive cache to determine a most finished cached element representing a display image satisfying the rendering request, the progressive cache including a plurality of caches arranged to store cached elements in a least finished to most finished order, there being one cache associated with each stage

(column 7 lines 33-45 and Figure 7 describe that all intermediate nodes can cache their processed image data, based on user specified caching requirements. Each intermediate node has a corresponding cache that receives an output element of a corresponding processing, or rendering, stage and can deliver this information to the next processing node in the processing pipeline upon request. This arrangement of caches is considered a progressive cache as caches corresponding to earlier processing stages, such as the cache associated with node 609 (Figure 6) contain the least processed, or least finished, cache elements, and caches corresponding to later processing stages, such as the cache associated with node 602, contain the most processed, or most finished, cache elements. Figure 5 and column 5 lines 22-35 describe the stages involved in processing an image); sending the most finished cached element to a starting stage of a rendering pipeline for the object, the starting stage being a next stage of the rendering pipeline corresponding to the most finished cached element (column 10 lines 46-58 describes that in rendering an image the process starts with the output node and works its way backwards through the processing nodes looking for cached data. If no cached data exists then the processing pipeline must begin processing the image from its initial state, but if cached data does exist then the search stops and the cached information is sent to the next stage in the processing pipeline for further processing. This is considered sending information from the progressive cache to the processing pipeline in the order from most finished cache element to the next stage after the corresponding stage, as the process starts with the output and works its way backwards through the processing stages looking for valid

cached information to send to the next stage in the processing pipeline); and sending an output of the starting stage to an input of a next stage of the rendering pipeline, a final stage of the rendering pipeline determining the display image satisfying the rendering request (column 7 lines 51-67, column 8 lines 1-11, and Figure 8 describe node 808, which receives the output of node 806 and is a final stage of the processing pipeline determining the display image satisfying the rendering request. Node 806 is the first processing stage, or starting stage, for the cached information held at node 803, and its output acts as input for node 808, which is the next stage of the processing pipeline).

Regarding claim 2, Gaudette describes a method wherein an output of a stage of the progressive pipeline is sent to the progressive cache (column 7 lines 33-45 and column 8 lines 32-44 describe that the cache associated with each node has three states, read-only, read/write, and no reading or writing (effectively no cache). If a user sets the cache associated with each processing node to the read/write state then the system stores the output image data to the cache every time the output image data is altered at that node).

Concerning claim 3, Gaudette describes a method wherein the progressive cache comprises a set of caches (column 7 lines 33-45 and Figure 7 describe that all nodes between input node 701 and output node 704 are considered intermediate nodes, and each intermediate node has an associated cache. This is considered a progressive cache that comprises a set of caches).

With regard to claim 12, Gaudette describes a method wherein the progressive cache finds a cache element using hashing (column 8 lines 45-67 describes that each

node cache contains data for a user specified set of image frames. Each node has a tag corresponding to whether its cache has valid image data for a particular frame, and if a node indicates that its cache contains valid frame data then the system searches the cache to find the valid frame, which is considered accessing cached elements by hashing).

As to claims 14 and 15, Gaudette describes a method wherein the rendering pipeline comprises a sequence of stages, wherein a particular stage in the sequence of stages processes the rendering request (column 5 lines 23-35 and Figure 5 describe creating a complex scene by processing an input image or multiple input images using a sequence of several processing stages).

Regarding claim 21, Gaudette describes a method wherein the starting stage associated with the cached element is a next stage of a corresponding stage of a cache of the progressive cache containing the cached element (Figure 8 describes that the cached information at node 803 is passed to processing node 806 upon request, node 806 has a corresponding cache, and node 806 and its associated cache are considered a starting stage and the next stage of the progressive cache for node 803 and its associated cache).

Concerning claim 22, Gaudette describes an apparatus for rendering, comprising: means for querying a progressive cache to determine a cached element most representing a display image satisfying a rendering request for an object (column 7 lines 51-67, column 8 lines 1-11, and Figure 8 describe caching image data at user specified nodes and then using the cached information that is furthest along in the

processing pipeline the next time the same frame is displayed to shorten the amount of required processing time. This is considered querying a progressive cache to determine a cached element most representing an output satisfying the processing request); means for sending the cached element to a starting stage of a rendering pipeline for the object, the starting stage associated with the cached element (Figure 8 describes node 806, which is the starting stage of the processing pipeline that receives the cached image information from node 803); and means for sending an output of the starting stage to an input of a next stage of the rendering pipeline, a final stage of the rendering pipeline determining the display image satisfying the rendering request (Figure 8 describes node 808, which receives the output of starting stage node 806 and is a final stage of the processing pipeline determining the output satisfying the processing request).

As to claim 23, Gaudette describes a system for rendering, comprising: a rendering pipeline including a plurality of stages connected serially to each other so that output of a previous stage provides input to a next stage, and a first stage is configured to receive a rendering request for an object, and a last stage is configured to produce a display image corresponding to the object (column 1 lines 66-67, column 2 lines 1-17, and Figure 6 describe a processing, or rendering, pipeline. Figure 6 illustrates input clips 603 through 606 and processing stages 607 through 610, which are configured to receive input clips 603 through 606 upon receipt of an input frame request, processing stages 609, 612, 613, and 602, which are connected serially to each other so that an output element of a previous stage is sent as an input to the next stage, and stage 601,

which is configured to produce an output corresponding to the input); a progressive cache including a plurality of caches arranged to store cached elements in a least finished to a most finished order (column 7 lines 33-45 and Figure 7 describe that all intermediate nodes can cache their processed image data, based on user specified caching requirements. Each intermediate node has a corresponding cache that receives an output element of a corresponding processing stage and can deliver this information to the next processing node in the processing pipeline upon request. This arrangement of caches is considered a progressive cache as caches corresponding to earlier processing stages, such as the cache associated with node 609 (Figure 6) contain the least processed, or least finished, cache elements, and caches corresponding to later processing stages, such as the cache associated with node 602, contain the most processed, or most finished, cache elements. Figure 5 and column 5 lines 22-35 describe the stages involved in processing an image); and a cache controller configured to route a most finished cached element from the progressive cache to a next stage of a corresponding stage of the rendering pipeline (column 10 lines 46-58 describes that in rendering an image the process starts with the output node and works its way backwards through the processing nodes looking for cached data. If no cached data exists then the processing pipeline must begin processing the image from its initial state, but if cached data does exist then the search stops and the cached information is sent to the next stage in the processing pipeline for further processing. This is considered sending information from the progressive cache to the processing pipeline in the order from most finished cache element to the next stage after the

corresponding stage, as the process starts with the output and works its way backwards through the processing stages looking for valid cached information to send to the next stage in the processing pipeline) and the output of a stage of the rendering pipeline to a corresponding cache of the progressive cache (column 10 lines 24-46 and Figure 12 describe an algorithm for accessing cache corresponding to a node. If a user has specified that a cache corresponding to a processing node is readable and writable then the algorithm, or cache controller, will route the processed image data to the cache to be stored. This process is carried out for every node in the processing pipeline. Thus, the algorithm is considered a cache controller that routes cache elements from the processing pipeline to the cache in the order from least finished cache elements to most finished cache elements, as it stores least finished cache elements in the cache that is associated with the first set of processing nodes (607 through 610, of Figure 6), based on user specified caching requirements, and progressively works its way through the pipeline caching processed data until it caches the most finished cache elements associated with the last set of processing nodes (node 602), based on user specified caching requirements).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-10 and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaudette et al. (US 6,867,782) in view of Dawson (US 6,567,099).

Regarding claims 4-8 and 16-20, Gaudette describes a rendering, or processing, pipeline and an associated progressive cache, as described in the rejection of claim 1. Gaudette doesn't describe a method wherein a particular cache in the set of caches is a preprocessed shape descriptor cache, a distance field cache, a distance values cache, an antialiased intensities cache, or a colorized image cache, and he doesn't describe a method wherein a particular stage in the sequence of rendering stages determines a preprocessed shape descriptor, determines a distance field, determines distance values, determines antialiased intensities, or determines a colorized image.

However, Dawson describes an anti-aliasing system comprising a polygon rendering system that receives geometric data for an image being rendered (column 3 lines 25-32). Dawson describes that the system receives geometric data and sends it to a rasterizer unit for processing. The rasterizer unit processes the image and stores the pixel data in a main buffer for later display. When the rasterizer unit processes geometric data for pixels located on an edge of an object in the image it stores higher resolution pixel data in an additional memory that has sufficient space to accommodate

the larger amount of incoming data (column 3 lines 33-67 and column 4 lines 1-2). The rasterizer unit contains a bit flag cache that signals to a memory controller whether to store low-resolution pixel data to the main buffer or high-resolution pixel data to the additional memory. The main buffer stores three pieces of information for each pixel: bit flag information, color data information, and z-distance information. If the bit flag is a one then the same three types of information are stored in the additional memory for four (or some other number larger than one) sub-pixels that make up the original pixel. The main buffer then replaces the z-distance information with a memory offset value describing the location of the higher resolution data in the additional memory. Dawson offers an example that describes a two-bit flag that is used to accurately describe how to process and store each pixel in an image (Figure 3 and column 7 lines 1-56). The example describes that the most significant bit in the flag represents a distance value, specifically whether the pixel is in the background or the foreground, and the least significant bit represents the high-resolution flag, indicating that a higher resolution version of the pixel should be stored in the additional memory. An average color of the sub-pixels that are determined to be in the foreground of original pixel is calculated while the sub-pixel information is stored in the additional memory and this average value is sent back to the main buffer to be stored as the color data for the corresponding main pixel (column 8 lines 45-57). The effect of calculating a more accurate color for the pixels that make up the edges of a foreground object is that visual aliasing of the object is significantly reduced.

It would have been obvious to one of ordinary skill in the art at the time of the invention to include in Gaudette the anti-aliasing method of rendering a graphic object, as taught by Dawson, in order to give the user the ability to add graphics to an image that don't exhibit a significant amount of aliasing. The advantage of adding graphics that don't exhibit a significant amount of aliasing is that the composite image looks more professional, as the transitions between layers in the composite image are well defined due to the minimal amount of aliasing.

Specifically addressing the limitations found in claims 4-8 and 16-20, the first stage in the rendering pipeline would receive background and foreground image data for an image that will be combined with a frame of digital film material, also considered determining a preprocessed shape descriptor (column 3 lines 25-28). This information would be generically stored in the cache corresponding to the shape descriptor stage. The second stage of the rendering pipeline would determine if a pixel in the graphic image is an edge pixel or a low-resolution background or foreground pixel, also considered determining a distance field for a pixel (column 7 lines 21-26). This information, in combination with the preprocessed shape descriptor information, would be stored in the cache corresponding to the distance field stage. The third stage would store the background and foreground information for all the low-resolution pixels in the main buffer, also considered determining distance values for the low-resolution pixels (column 7 lines 27-42). All processed information would be stored in the cache corresponding to the distance values stage. The fourth stage would store the high-resolution edge pixels to the additional memory and determine which sub-pixels are part

of the background and which sub-pixels are part of the foreground. The colors of all the sub-pixels that are determined to be part of the foreground are blended to create an average color and the distance values are combined and represented by one distance value that indicates that the pixel is part of the foreground, also considered determining antialiased intensities for the pixels that make up the edges of the foreground object (column 7 lines 43-56 and column 8 lines 42-57). All processed information would be stored in the cache corresponding to the antialiased intensities stage. Finally, in the fifth stage the average color and the distance value of the pixels that make up the edges of the foreground object would be written back to the main buffer and the main buffer would output the color triplet data for all pixels to the display, along with any underlying digital film data. This is considered determining a colorized image (column 8 lines 58-67 and column 9 line 1). The output information would be stored in the cache corresponding to the colorized image stage.

As to claim 9, Gaudette in view of Dawson describes a method wherein distance values for a component of a pixel of the display image are stored in the distance values cache (Dawson column 7 lines 27-42 describes a flag that defines whether the pixel is a foreground pixel or a background pixel, which is considered a distance value that represents the pixel. Given the scenario described in the rejection of claims 4-8 and 16-20, the determined distance value for each low-resolution pixel is stored in the associated distance values cache).

Regarding claim 10, Dawson describes a method wherein the distance values for the component of the pixel of the display image are combined prior to determining an

antialiased intensity for the component of the pixel (column 8 lines 42-57 describes that all the color values of the foreground sub-pixels are averaged and this average value is used to represent the entire pixel. Once the average color is determined the background and foreground distance values are combined into one distance value, which indicates that the pixel is a foreground pixel. Combining the distance values to convert the sub-pixels into one foreground pixel is considered the last step before the antialiased intensity (the color, in this case) is sent back to the main buffer to replace the old color value representing the main pixel).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gaudette et al. (US 6,867,782) in view of Naffziger et al. (US 6,640,283).

Concerning claim 11, Gaudette describes a rendering pipeline where each stage of the pipeline has a corresponding cache, as described in the rejection of claim 1. Gaudette doesn't describe a system or method wherein the cached elements are compressed.

However, Naffziger describes a system and method for compressing cached elements (column 4 lines 36-44). It would have been obvious to one of ordinary skill in the art at the time of the invention to include in Gaudette the system and method of compressing cached data, as taught by Naffziger, in order to enable the storage of additional data within the same amount of area, which allows more frames of data to be stored in each cache in the system described in Gaudette. The advantage of storing more frames of data is that the system will have to process less unchanged information when outputting a sequence of frames, which means the system will be able handle a

larger processing load of new information without lengthening the associated processing time.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gaudette et al. (US 6,867,782) in view of Robertson et al. (US 5,956,744).

As to claim 13, Gaudette describes a rendering pipeline where each stage of the pipeline has a corresponding cache, as described in the rejection of claim 1. Gaudette also describes that as cache space runs low the system uses a set of criteria to determine which portion of cache is not needed and should be overwritten (column 10 lines 59-67 and column 11 lines 1-40 describe prioritizing portions of cache based on number of times the cache is accessed, proximity to the output node, and other criteria). Gaudette doesn't describe a system or method wherein least recently used cache elements are discarded when the progressive cache is full.

However, Robertson describes a system and method in which the least recently used cached elements are discarded when the progressive cache is full (column 5 lines 60-67 and column 6 lines 1-24). It would have been obvious to one of ordinary skill in the art at the time of the invention to include in Gaudette the system and method of discarding the least recently used cache elements, as taught by Robertson, in order to add the least recently used criterion to the set of criteria for replacing cache data disclosed in Gaudette. The advantage of adding the least recently used criterion to the set of criteria disclosed in Gaudette is that the system will be able to better predict the least valuable cache, which makes the use of cache space more efficient.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Cai et al. (US 6,470,422), Casamatta (US 6,243,794), and Deshpande et al. (US 6,442,597) describe multiprocessor multi-cache systems, and Singh et al. (US 6,324,621) describes a method of cache compression.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Washburn whose telephone number is (571) 272-5551. The examiner can normally be reached on Monday through Friday 8:30 a.m. to 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on (571) 272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DW

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3/21/06

Ulka Chauhan

ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER